

Appl. No. 10/710,175
Amdt. dated November 25, 2005
Reply to Office action of August 26, 2005

Amendments to the Claims

Listing of Claims:

- 5 Claim 1 (currently amended): An apparatus for generating a phase delay, comprising:
 a buffer for buffering an input signal and outputting an output signal;
 a DAC for outputting a control voltage corresponding to a digital value
 representative of a phase delay; and
 a variable capacitor coupled to the DAC and the buffer, the capacitance value
10 of the variable capacitor corresponding to the control voltage, the variable
 capacitor being a P+/N well junction voltage-controlled capacitor;
 wherein by controlling the capacitance value, the apparatus adjusts the phase
 delay between the input signal and the output signal.
- 15 Claims 2-6 (cancelled)
- Claim 7 (currently amended): A method for generating a phase delay comprising the
 following steps:
 buffering an input signal to generate an output signal;
20 providing a digital value representative of a phase delay;
 generating a control voltage corresponding to the digital value representative of
 the phase delay; and
 adjusting a capacitance value of a variable capacitor with the control voltage, to
 adjust the phase delay between the input signal and the output signal,
25 wherein the variable capacitor is a P+/N well junction voltage-controlled
 capacitor.

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Claims 8-13 (cancelled)

Claim 14 (new) : An apparatus for adjusting a phase difference between two input

signals, the apparatus comprising:

- 5 a first buffer for buffering a first input signal and outputting a first output
 signal;
- a first DAC for outputting a first control voltage corresponding to a first digital
 value representative of a phase delay;
- 10 a first variable capacitor coupled to the first DAC and the first buffer, the
 capacitance value of the first variable capacitor corresponding to the first
 control voltage;
- a second buffer for buffering a second input signal and outputting a second
 output signal;
- 15 a second DAC for outputting a second control voltage corresponding to a
 second digital value representative of a phase delay; and
- a second variable capacitor coupled to the second DAC and the second buffer,
 the capacitance value of the second variable capacitor corresponding to
 the second control voltage;
- 20 wherein by controlling at least one of the first and the second digital values, the
 phase difference between the first input signal and the second input signal
 are adjusted.

Claim 15 (new) : The apparatus of claim 14 being implemented in a receiver.

25 Claim 16 (new) : The apparatus of claim 14 being implemented in a transmitter.

Claim 17 (new) : The apparatus of claim 14 being implemented in a transceiver.

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Claim 18 (new) : The apparatus of claim 14, wherein the first input signal and the second input signal are differential signals.

- 5 Claim 19 (new) : The apparatus of claim 14, wherein the first input signal and the second input signal are an in-phase signal and a quadrature-phase signal respectively.

- 10 Claim 20 (new) : The apparatus of claim 14, wherein the first input signal and the second input signals are clock signals.

Claim 21 (new) : The apparatus of claim 14, wherein the first input signal and the second input signal are RF signals.

- 15 Claim 22 (new) : The apparatus of claim 14, wherein the first variable capacitor and the second variable capacitor are voltage-controlled capacitors.

20 Claim 23(new): The apparatus of claim 22, wherein the voltage-controlled capacitors are MOS-based voltage-controlled capacitors.

Claim 24(new): The apparatus of claim 22, wherein the voltage-controlled capacitors are P+/N well junction voltage-controlled capacitors.

- 25 Claim 25 (new) : A method for adjusting a phase difference between two input signals, the method comprising:
buffering a first input signal and outputting a first output signal;
buffering a second input signal and outputting a second output signal;

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providing at least one of a first digital value and a second digital value
representative of a first phase delay and a second phase delay respectively;
and
adjusting a first capacitance value of a first variable capacitor with a first
5 control voltage generated from the first digital value or adjusting a second
capacitance value of a second variable capacitor with a second control
voltage generated from the second digital value, to adjust the phase
difference between the first input signal and the second input signal.

10 Claim 26 (new) : The method of claim 25, wherein the first input signal and the
second input signal are differential signals.

Claim 27 (new) : The method of claim 25, wherein the first input signal and the
second input signal are an in-phase signal and a quadrature-phase signal
15 respectively.

Claim 28 (new) : The method of claim 25, wherein the first input signal and the
second input signals are clock signals.

20 Claim 29 (new) : The method of claim 25, wherein the first input signal and the
second input signal are RF signals.

Claim 30 (new) : The method of claim 25, wherein the first variable capacitor and the
second variable capacitor are voltage-controlled capacitors.

25 Claim 31 (new) : The method of claim 30, wherein the voltage-controlled capacitors
are MOS-based voltage-controlled capacitors.

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Claim 32 (new) : The method of claim 30, wherein the voltage-controlled capacitors
are P+/N well junction voltage-controlled capacitors.

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